In response, however, Applicants submit that all such informal matters have now been corrected pursuant to the above-noted amendment to independent claim 1. As such, the §112 rejection is now obviated.

In paragraphs 5 through 7 of the Final Office Action, the Examiner rejected claims 1, 3, 4, 6 and 17 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,357,622 to Magdo et al., U.S. Patent No. 4,038,680 to Yagi et al. or U.S. Patent No. 5,529,939 to Lapham et al. In light of the above-noted amendments, however, Applicants respectfully submit that the claims of the present invention, as amended, are both novel and non-obvious over such references.

Specifically, independent claim 1 has now been amended so as to include the limitation that "said second embedded diffusion layer is a terminal of said second vertical type high voltage NPN bipolar transistor." This limitation, again along with the fundamental limitation of requiring the combination of a high speed NPN bipolar transistor with a high voltage NPN bipolar transistor, is not taught, suggested nor even contemplated by any of the cited references.

Indeed, the primary reference cited by the Examiner, Magdo, is specifically directed to producing complementary PNP and NPN transistor pairs on a common substrate having matched high performance characteristics, and wherein it is desirable to provide a barrier for one of the transistor pairs which does not act to provide a secondary PN junction. Accordingly, Applicants submit that it is erroneous to conclude that it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second NPN transistor in the Magdo device because it is conventional in the art to reverse the polarity of a transistor, since Magdo is *specifically directed* to complementary PNP and NPN transistor pairs.

Moreover, the "second embedded diffusion layer 18" cited by the Examiner from the Magdo reference is not, in fact, an embedded diffusion layer as in the present invention. Rather, it is a "barrier region" which is specifically formed between the associated bipolar transistor and the substrate so as to electrically separate the two layers. Accordingly, the barrier layer 18 of Magdo *cannot* work as a collector, or any terminal, of the bipolar transistor.

Conversely, the second embedded diffusion layer of the present invention serves as an effective collector of the second vertical type high voltage NPN bipolar transistor. As a result of this specific arrangement, the associated breakdown voltage of the transistor may be improved.

Applicants respectfully submit that none of the references cited by the Examiner, particularly the Magdo reference, either alone or in combination with each other, teach or suggest the specific combination of a first vertical type high speed NPN bipolar transistor with a second vertical type high voltage NPN bipolar transistor on a single semiconductor substrate in a semiconductor device wherein a second embedded diffusion layer of the second vertical type high voltage NPN bipolar transistor is a terminal of such transistor.

Accordingly, Applicants respectfully request that the claims as herein proposed be deemed allowable.

It is further submitted that no fees are due in connection with this application, the office is authorized to deduct said fees from Deposit Account No. 08-2290. If such a withdrawal is made, please indicate the Attorney Docket No. (P97,2608) on the account statement.

Respectfully submitted,

(Reg. No. 39,056)

William E. Vaughan
HILL AND SIMPSON
A Professional Corporation
85th Floor Sears Tower
Chicago, Illinois 60606
(312) 876-0200
Attorneys for Applicants

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents Washington, D.C. 20231 on December 14, 1999.